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4H-SiC oxynitridation for generation of insulating layers

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Abstract

This paper describes the present state of a nitrogen-based passivation for SiO_2 layers on 4H-SiC. Interface state density, oxide breakdown field, channel mobility and gate oxide reliability have been characterized following nitric oxide (NO) passivation anneals. The kinetics of nitrogen incorporation and the quantitative modelling between nitrogen content and interface trap density with NO anneals have also been discussed.

1. Introduction

Silicon carbide is a promising semiconductor for high power, high temperature and high frequency devices because of superior material properties [1] such as large band gap, high thermal conductivity, high breakdown field strength and high saturated electron drift velocity. SiC is the only compound semiconductor that has a native oxide (silicon dioxide) that can be used to fabricate standard MOS device structures. The 4H polytype has a larger band gap energy and a higher, more isotropic electron mobility, and is therefore the polytype of choice for high power applications. Silicon carbide *n*-channel inversion-mode MOSFETs have been fabricated with both the 4H and 6H polytypes [2, 3]. Blocking voltages for 4H-SiC MOSFETs have been improved significantly with thicker epitaxial layers and better edge terminations; however, the on-resistance of these devices is still very high and is currently dominated by the high inversion channel resistance due to the low channel mobility. The high channel resistance severely limits the current handling capability (and as a result the power handling capability) of the device.

The channel mobility is affected by several parameters such as interface trap density, surface roughness and effective field normal to the interface. The low channel mobility of 4H-SiC MOSFETs has been linked to a large, broad interface state density located at approximately

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2.9 eV above the valence band edge. This interface state density (D_{it}) exists in both 4H and 6H polytypes of SiC [4]. For 6H-SiC ($E_{gap} \sim 3$ eV), these localized states lie mostly in the conduction band, and hence have little effect on inversion channel mobility. However for 4H-SiC ($E_{gap} \sim 3.3$ eV), the interface states lie mostly in the band gap where they act to reduce channel mobility through field termination, carrier trapping and Coulomb scattering. High integrated interface state densities of the order of 10^{13} cm^{-2} have been observed for both n- and p-4H-SiC [5–7]. These states are believed to result from carbon clusters that remain at the interface and from defects in a near-interface sub-oxide that is produced when the oxidation process is terminated [8, 9].

A number of different approaches have been undertaken to improve the *n*-channel mobility for 4H-SiC MOSFETs. Sridevan and Baliga [10] reported effective mobilities as high as 128 cm^2 V^{-1} s^{-1} for deposited oxides that were annealed sequentially in wet nitrogen at 1100 °C, argon at 1100 °C and wet nitrogen at 950 °C. However, these results have not been widely duplicated. Ogino *et al* [11] used low dose nitrogen implants in the *n*-channel region to control threshold voltages and reported higher mobilities (∼99 cm^2 V^{-1} s^{-1}) following implantation. Fukuda *et al* [12, 13] reported improvements in the interface characteristics with hydrogen annealing at temperatures above 800 °C and claimed the termination of the dangling bonds of Si and carbon by hydrogen. Promising results have also been obtained by Yano *et al* [14] who reported effective channel mobilities of approximately 30 cm^2 V^{-1} s^{-1} and low field mobilities of around 90 cm^2 V^{-1} s^{-1} following oxidation of the (11$\bar{2}$0) surface (the a-face) of 4H-SiC. (The low field mobilities were calculated using analysis techniques that eliminate the source/drain contact resistance as a source of error [15].) They claim that the problem of low channel mobility in 4H-SiC MOSFETs can be solved using (11$\bar{2}$0) substrates. Senzaki *et al* [16] used hydrogen annealing at 800 °C with (11$\bar{2}$0) 4H-SiC substrates and reported a higher channel mobility of around 110 cm^2 V^{-1} s^{-1}.

Li *et al* [17] reported improvements in the interface characteristics of 6H-SiC MOS capacitors following high temperature anneals in nitric oxide (NO). Jamet *et al* [18, 19] proposed a nitridation model for oxides grown or annealed in N_2O and NO, and claimed that Si–N bonding and carbon removal at the interface account for the observed beneficial effects. Lipkin *et al* [20] also used N_2O for oxide growth and for post-oxidation anneals of thermal oxides and reported effective channel mobilites around 20–25 cm^2 V^{-1} s^{-1}. We have optimized post-oxidation NO anneals for 4H-SiC to develop a passivation process that reduces the interface state density near the conduction band edge by more than one order of magnitude for n-4H-SiC MOS capacitors [21]. We attribute the reduction in the interface state density to the passivation of carbon cluster or silicon suboxide states that have energies in the top half of the SiC band gap. Nitrogen introduced during the NO passivation anneal reacts with defects to shift their energies into the lower half of the band gap. We have also carried out passivation anneals with ammonia (NH_3) [22], post metallization anneals (PMAs) with Mo and Al gate electrodes [23], and passivation anneals using forming gas (N_2/5% H_2) [24]. PMAs showed no improvement for the interface state density. Anneals in forming gas at temperatures up to 1000 °C resulted in an improvement of about a factor of two for D_{it} at $E_c - E = 0.6$ eV; however, at 0.15 eV below the conduction band edge, no noticeable improvement was observed. Ammonia appears to be just as effective as NO in reducing $D_{it}(E_c)$; however, breakdown field strengths were found to be much lower for oxide layers passivated with NH_3. We attribute the lower breakdown field strengths to the fact that nitrogen appears uniformly throughout the oxide layer as well as at the SiC/SiO_2 interface following NH_3 anneals, while nitrogen accumulates almost entirely at the interface following NO passivation anneals [25]. Furthermore, for similar anneal conditions, the amount of incorporated nitrogen is approximately 100 times higher for NH_3 compared to NO. We also used N_2O for post-oxidation anneals at temperatures between

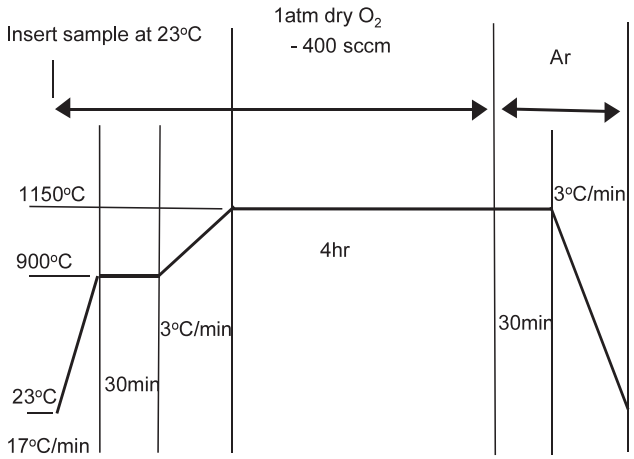

Figure 1. Standard thermal dry oxidation process.

1050 and 1175 °C; however, the interface characteristics did not improve [26]. We proposed that higher oxygen partial pressure contributes to the growth of additional oxide, thereby creating competition between fresh oxide growth and defect passivation by nitrogen.

Considering both interface state passivation and oxide breakdown, we have achieved our best results using nitric oxide. However, the origin of defects at the 4H-SiC/SiO_2 interface and the role of nitrogen in the passivation process are still widely debated, and efforts continue to model the interface and to improve it for device applications. In this paper, we present results for interface state density, channel mobility and oxide reliability for 4H-SiC MOS capacitors and lateral MOSFETs processed with the NO passivation anneal.

2. Sample preparation

5–10 μm 4H-SiC epilayers ($N_d = (4–8) \times 10^{16}$ cm^{-3}) were oxidized using standard techniques for dry oxidation and the temperature profile shown in figure 1. Following oxidation to produce 30–40 nm oxide layers, the samples were annealed in a second furnace in NO at 1175 °C for 2 h. Gas flow was maintained at 0.41 min^{-1} at a pressure of 1 atm during the post-oxidation anneals. Following these anneals, Mo was sputter-deposited to form oxide gate contacts, and large area backside ohmic contacts were formed to the N^+ substrates using Ag colloidal paste. Standard high frequency (1 MHz)–low frequency (quasi-static) capacitance–voltage techniques were applied to characterize the SiO_2/n-4H-SiC MOS capacitors. *N*-channel planar MOSFETs were fabricated on p-4H epilayers ($N_a = (2–5) \times 10^{15}$ cm^{-3}) with the same oxidation process used for the MOS capacitors. Heavily doped source/drain regions were formed with multiple energy nitrogen ion implants at 700 °C. The implants were activated with post-implant anneals at 1575 °C for 30 min in flowing Ar. Molybdenum was deposited to form gate electrodes for lateral devices that had channel lengths and widths of 200 and 300 μm, respectively. The planar MOSFETs were characterized with an HP 4145A semiconductor parameter analyser connected to a Signatone high temperature probe station. The temperature was controlled with a Signatone temperature controller calibrated to a set point accuracy of 1 °C.

High temperature oxides (HTOs) were deposited at 950 °C using standard techniques that included a post-deposition 're-oxidation' anneal in dry N_2 at 950 °C for 1 h. Low temperature oxides (LTOs) were deposited at 300 °C by PECVD. Current–voltage and charge injection

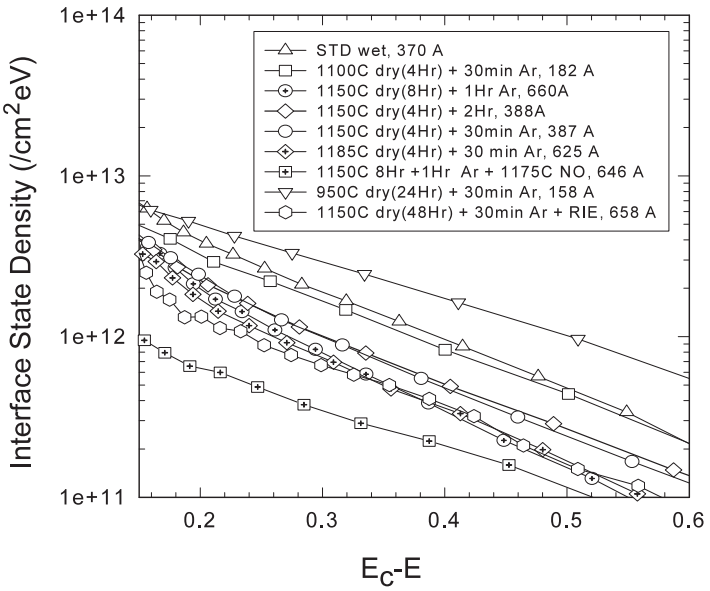

Figure 2. Interface state densities for oxides on 4H-SiC for various oxidation times and temperatures.

measurements were performed at room temperature and at 290 °C using Keithley 4200 SCS and 2410-20 SMU systems.

3. Experimental results and discussion

3.1. Dry, thermal oxides passivated with NO

The results of D_{it} measurements at room temperature for 4H-SiC MOS capacitors with dry oxides before and after NO anneals are shown in figure 2. Although D_{it} values from Hi–Lo C–V measurements may be quite uncertain so close to E_c, the relative values are reliable and clearly indicate the trend. 'STD wet' refers to samples that were oxidized with our standard wet oxidation procedures at 1100 °C [23], and the numbers in the legends are oxidation temperature, time and oxide thickness. Dry oxides have lower oxidation rates and interface state densities near the conduction band compared to wet oxides grown at the same temperature. For a given oxidation temperature, the interface state density near the conduction band ($D_{it}(E_c)$) does not change when the time of the post-oxidation Ar anneal is varied. Chang *et al* [27] associated low D_{it} values for oxides grown at 950 °C with a minimum concentration of carbonaceous species and a reduced transition layer thickness in 6H-SiC. However, our dry oxides grown at 950 °C on 4H-SiC were found to have the highest $D_{it}(E_c)$ values of any of the samples that were measured. With increasing oxidation time or temperature, the oxide thickness increases, and $D_{it}(E_c)$ decreases. For dry oxides grown at 1150 °C for 48 h, the original oxide thickness was around 400 nm. Thinner oxide layers in figure 2 were obtained by reactive ion etching the original 400 nm layers. NO passivation produced the same D_{it} numbers for all samples regardless of oxidation time and temperature; hence, results are plotted in figure 2 only for samples oxidized at 1150 °C.

Power DIMOSFETs or UMOSFETs are fabricated with oxide layers grown on implanted/activated or etched SiC surfaces, and the interface state density is an important

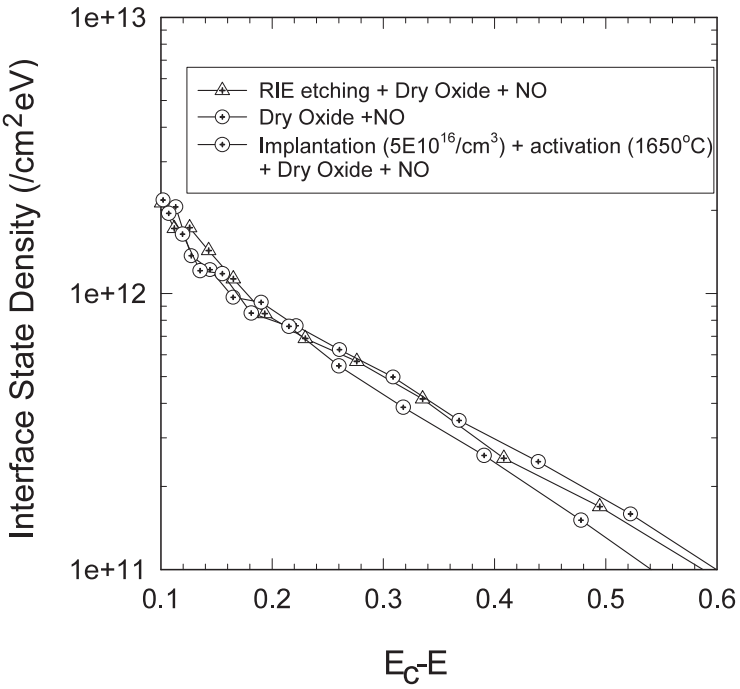

Figure 3. Interface state densities for dry thermal oxides on implanted 4H-SiC ($\sim 5 \times 10^{15}$ cm^{-2} in the *n*-channel region) and on 4H-SiC samples that were reactively ion etched in pure NF_3.

property of the surfaces. Figure 3 shows interface state densities for dry oxides grown on implanted/activated and etched 4H-SiC. Several samples were reactively ion etched using pure NF_3 to remove about 500 nm of the SiC epilayers prior to dry oxide growth and subsequent NO passivation. Etched and standard samples were found to have the same interface state densities following passivation. Other samples were implanted with Al at a concentration of 5×10^{16} cm^{-3} in the channel area and activated at 1650 °C for 30 min in Ar in a SiC pillbox prior to dry oxidation and passivation. The implanted/activated sample shows same interface state density as the standard and the etched samples following the NO passivation anneals.

3.2. Deposited oxides passivated with NO

Deposited oxides on 4H-SiC may have different interface characteristics compared to thermal oxides. We have prepared high temperature and low temperature deposited oxides and passivated the oxide/SiC samples with post-deposition NO anneals. Figure 4 shows the interface state density for HTO and LTO samples as a function of trap energy relative to the conduction band edge. Results for our standard dry oxide are included for comparison. The HTO sample, processed with a re-oxidation anneal only, shows a very high interface state density ($\sim 5 \times 10^{13}$ cm^{-2} eV^{-1}) at a trap energy 0.1 eV below E_c. After NO passivation, $D_{it}(E_c)$ decreases to approximately 1×10^{12} cm^{-2} eV^{-1} at $E_c - E = 0.1$ eV. We could not make meaningful quasi-static C–V measurements for as-deposited LTO samples. These samples exhibited high leakage currents that reflect the poor quality of the LTOs. However, after NO annealing, all samples—LTO, HTO and thermal—have approximately the same trap density near the conduction band edge. After NO passivation, regardless of the method of

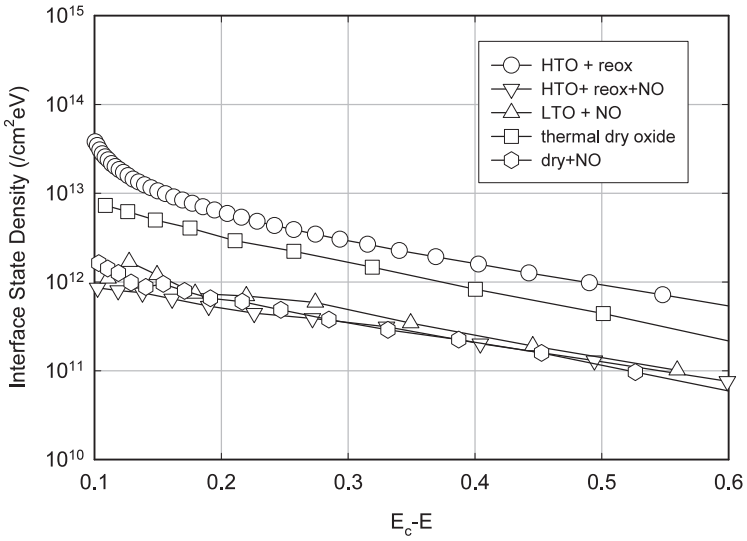

Figure 4. Interface state densities for deposited and dry thermal oxides on n-4H-SiC.

preparation, oxides on n-4H-SiC have similar interface state densities near the conduction band—typically around (1–2) $\times$ 10^{12} cm^{-2} eV^{-1} at $E_c - E = 0.1$ eV. In this work, we may assume that our LTO samples have much lower interfacial concentrations of carbon following deposition at 300 °C. However, we did not find the low interface state densities expected from such low carbon concentrations. This can be explained by assuming that additional oxide growth occurs during the NO passivation anneal. We have observed an increase in thickness of approximately 6% for a 40 nm oxide layer annealed in NO for 2 h at 1175 °C [28]. Therefore, regardless of the initial oxide deposition process, the passivation anneal produces a thin thermal oxide at the interface where defect passivation by nitrogen and defect generation as a result of the continuing oxidation are competing processes.

3.3. Oxide breakdown field strengths with NO anneal

Table 1 shows the results of current–voltage measurements carried out in order to study the effect of the passivation anneal on the breakdown characteristics of various oxides on 4H-SiC. The breakdown voltage was defined as the voltage at which the measured reverse current density reached 10^{-4} A cm^{-2}. The voltages used to calculate the breakdown field strengths were corrected for flatband shifts. The NO passivation anneal applied to the dry thermal oxide results in a significant improvement in breakdown performance at room temperature and at 290 °C. However, the passivated HTO samples had even higher breakdown fields at room temperature and at 290 °C. The lower breakdown fields of the LTO samples are likely the result of poor bulk properties that often characterize low temperature deposited oxides.

3.4. Planar 4H-SiC MOSFETs passivated with NO

Figures 5(a) and (b) show drain current (I_D)–drain voltage (V_D) characteristics at a constant gate voltage (V_G) of 10 V for 4H-SiC MOSFETs with dry thermal oxides before and after NO passivation. The devices exhibit excellent gate-controlled linear and saturation regimes of operation. At the onset of saturation, the drain current for MOSFETs without NO passivation

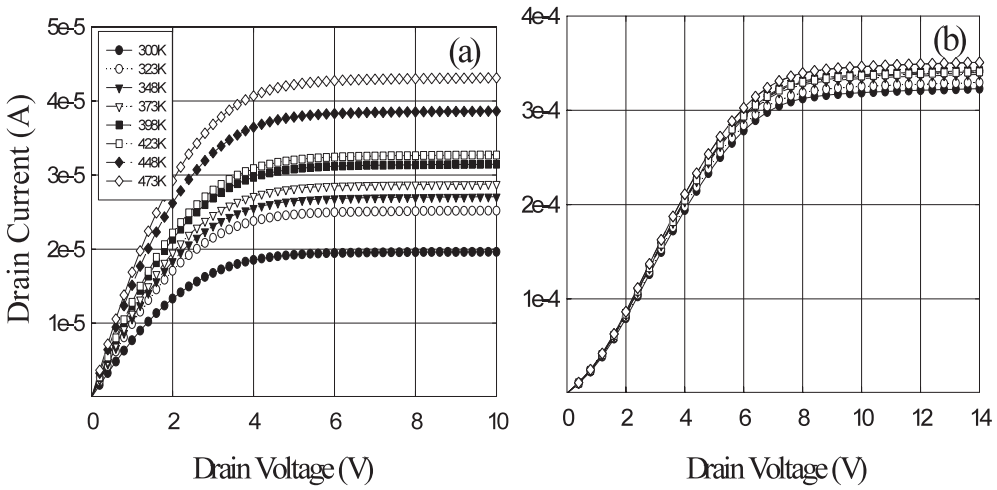

Figure 5. I_D–V_D characteristics at a constant V_G of 10 V for 4H-SiC MOSFETs without (a) and with (b) the NO passivation anneal.

Table 1. Breakdown characteristics for oxide layers on n-4H SiC.

Sample	E_{ave} (MV cm^{-1}) 23 °C (σ)	E_{max} (MV cm^{-1}) 23 °C	E_{ave} (MV cm^{-1}) 290 °C (σ)	E_{max} (MV cm^{-1}) 290 °C
Dry thermal oxide + NO	9.5 (0.7)	10.7	7.7 (1.3)	9
Wet thermal oxide + NO	9.9 (0.2)	9.7	5.4 (0.9)	5.6
HTO + Reox + NO	10.4 (0.9)	11.8	8.0 (1.5)	9.8
LTO + NO	3.3 (1.8)	4.2	1.8 (1.3)	2.4

increases from 0.02 to 0.04 mA with increasing temperature from 300 to 473 K. For the NO-passivated MOSFET, the drain current increases from 0.32 to 0.35 mA over the same temperature range.

Figure 6 shows room temperature field effect channel mobilities (μ_{eff}) as a function of gate voltage for passivated and unpassivated MOSFETs. The effective mobility was calculated using standard techniques [29] and a drain voltage V_D of 0.05 V. The device has a peak channel mobility of approximately 35 cm^2 V^{-1} s^{-1}, and shows a 14× improvement in peak mobility as a result of the NO passivation anneal. Lu *et al* [30] reported a peak channel mobility of 50 cm^2 V^{-1} s^{-1} using our NO anneal process. Our own devices show low field mobilities of approximately 100 and 8 cm^2 V^{-1} s^{-1}, respectively, with and without NO passivation. We also characterized our MOSFETs with and without source/drain contact anneals at 900 °C for 3 min in Ar. The field effect channel mobilities for the passivated and unpassivated devices did not change after anneals. At this time, we do not have a satisfactory explanation for why the field effect mobility is so much lower than the low field mobility. The maximum field effect mobilities as a function of temperature are shown in figure 7 for 4H-SiC MOSFETs with and without NO passivation. The field effect mobility of the unpassivated device increases with increasing temperature in proportion to $T^{1.9}$, while the mobility of the passivated MOSFET remains almost unchanged. Several previous studies [10, 31, 32] of 4H-SiC MOSFETs reported increasing mobility with increasing temperature. These observations were explained by the reduction in Coulomb scattering due to the thermal emission of electrons from the interface traps near the conduction band. However, Yano *et al* [33] recently reported that the mobility

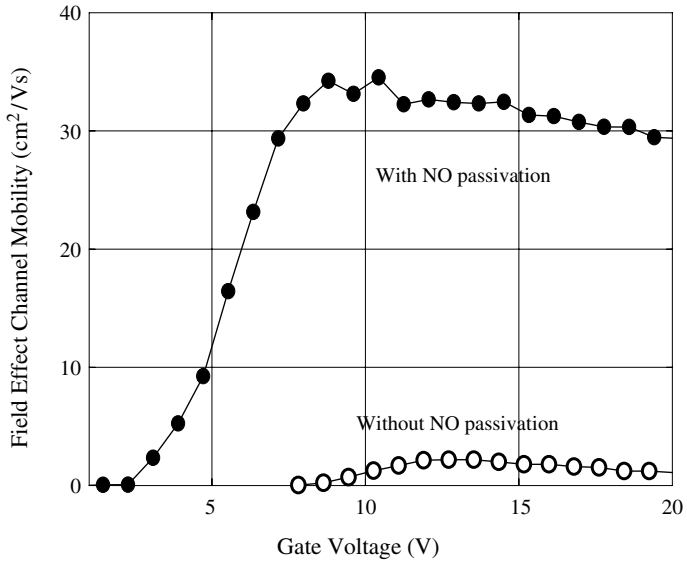

Figure 6. Field effect channel mobility for dry oxide 4H-SiC MOSFETs fabricated with and without NO passivation.

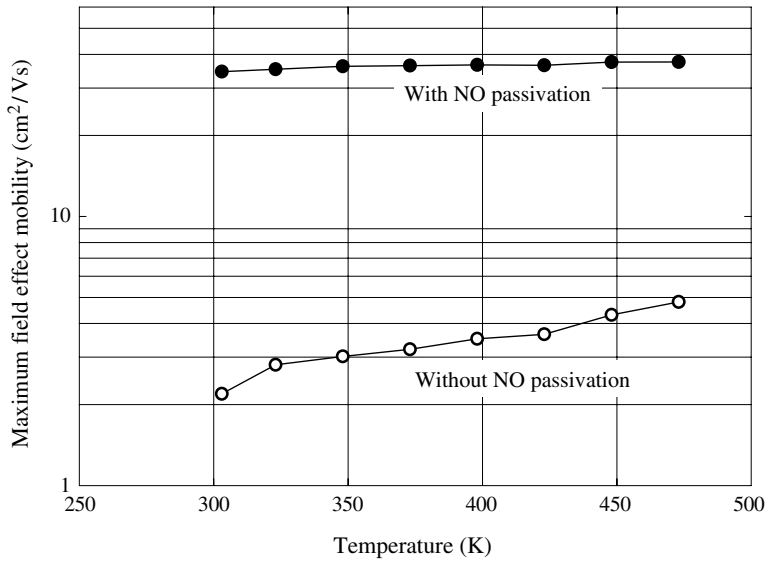

Figure 7. Temperature dependence of the maximum field effect mobility with and without NO passivation.

for MOSFETs fabricated on $(11\bar{2}0)$ 4H-SiC has a negative temperature dependence. They suggest that the a-face has lower unpassivated interface state density near the conduction band, so that carrier transport is more affected by phonon scattering—as is observed for Si MOSFETs. However, we have measured the interface state density near the conduction band using n-4H-SiC MOS capacitors and find that our NO-passivated MOSFETs have trap densities comparable to those reported by Yano. We speculate that, even with NO passivation, our interface state

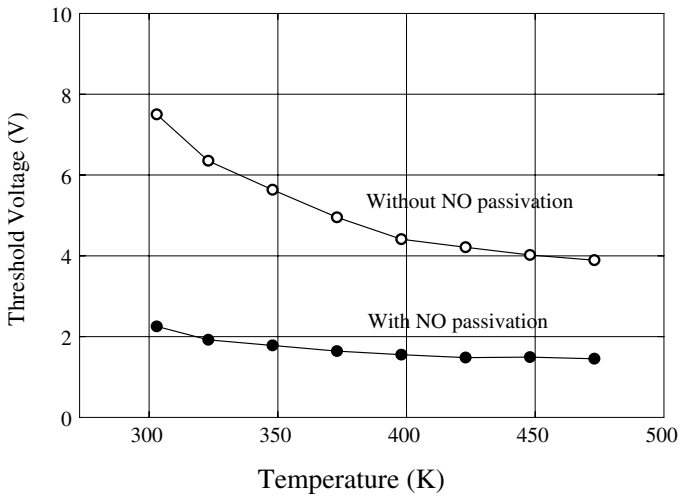

Figure 8. Temperature dependence of the threshold voltage with and without NO passivation.

density is still in the range where the Coulomb scattering affects carrier transport at least as much as phonon scattering.

Figure 8 shows the temperature dependence of the threshold voltage for 4H-SiC MOSFETs with and without NO passivation. Data were obtained using linear extrapolation techniques and I_D–V_G characteristics measured at $V_D = 0.1$ V. The threshold voltage of the unpassivated MOSFET decreases significantly from 7.5 to 3.9 V over the temperature range 300–473 K. However, the passivated MOSFET has only a weak temperature dependence for V_{th}. Decreasing threshold voltage corresponds to the reduction of negative effective charge in the oxide or at the interface for both passivated and unpassivated devices. The primary source of the negative charge is electrons trapped in acceptor-like interface states. The weak temperature dependence of V_{th} for the passivated MOSFET can be attributed to the lower number of acceptor-like interface states near the conduction band edge.

3.5. Oxide reliability following passivation with NO

In order to fabricate advanced SiC MOS power devices, oxide reliability must be improved. Several papers have reported the results of gate oxide lifetime measurements for SiC MOS devices [34–36]. The lifetime of the oxide strongly depends on charge trapping in the oxide during operation [37]. Recently, Arai *et al* [38] reported the results of 4H-SiC MOS reliability measurements using the constant current method. We have applied this technique to thermal and deposited oxides to determine the effect of NO passivation on oxide reliability.

Figure 9 shows high frequency C–V curves and charge injection times for a standard dry oxide (a), an NO annealed dry oxide (b), and an NO annealed high temperature deposited oxide (c). Hot electrons were injected from the 4H-SiC substrate at a constant current density of 4 μA cm^{-2} for times between 10 and 1200 s. The flat band voltages of all the oxides show positive shifts with increasing injection time. Negative charge trapping occurs in all the oxides, and the amount of trapped charge increases with increasing injection charge. Figure 10 shows the change in effective oxide charge (ΔQ_{eff}) for the oxides of figure 9. ΔQ_{eff} was defined as an absolute number that is the difference between the initial effective oxide charge and the oxide charge after charge injection. ΔQ_{eff} increases with increasing injection time up to

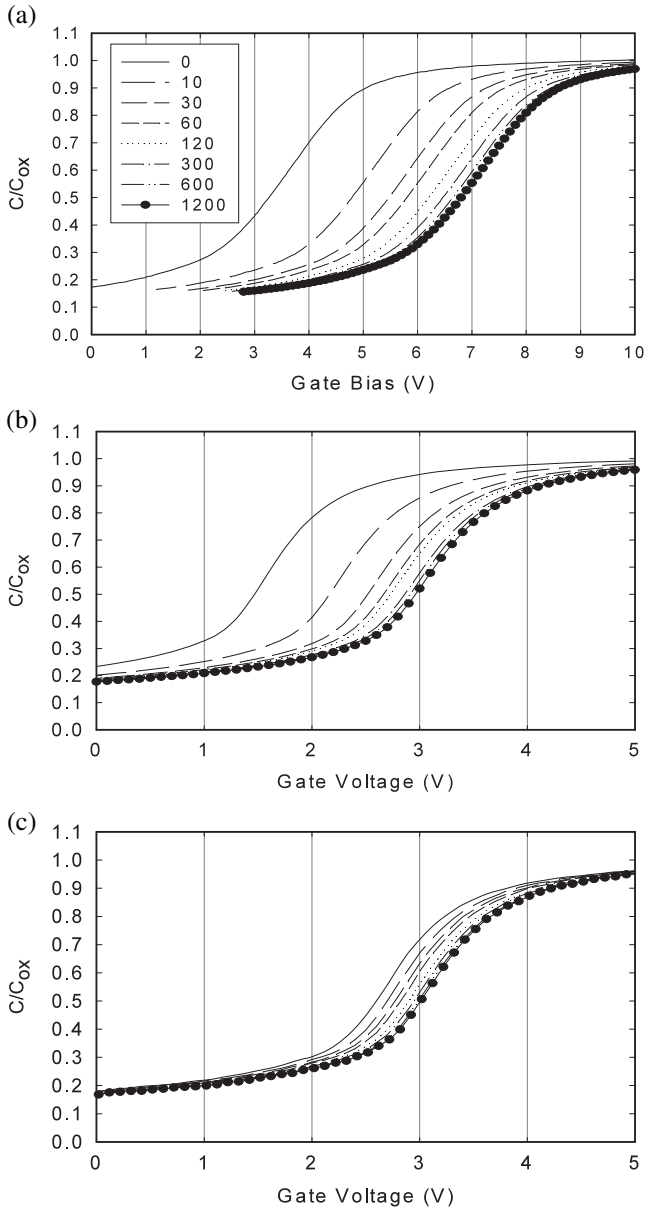

Figure 9. High frequency *C–V* curves for various charge injection times. (a) Dry oxide, (b) NO annealed dry oxide, (c) NO annealed HTO.

200 s, and then saturates for all three samples. The dry thermal oxide has a lower ΔQ_{eff} after NO annealing, and the NO annealed HTO shows the lowest ΔQ_{eff} over the whole range of injection times. Primarily, electron trapping with the charge injection is related with defects that exist in the oxide and at the interface [37]. Kosugi *et al* [39] reported improvements for hot-carrier tolerance due to the reduction of the interface state density in LTO gate oxides. We attribute the lower ΔQ_{eff} in the NO passivated oxides to the reduction of the interface

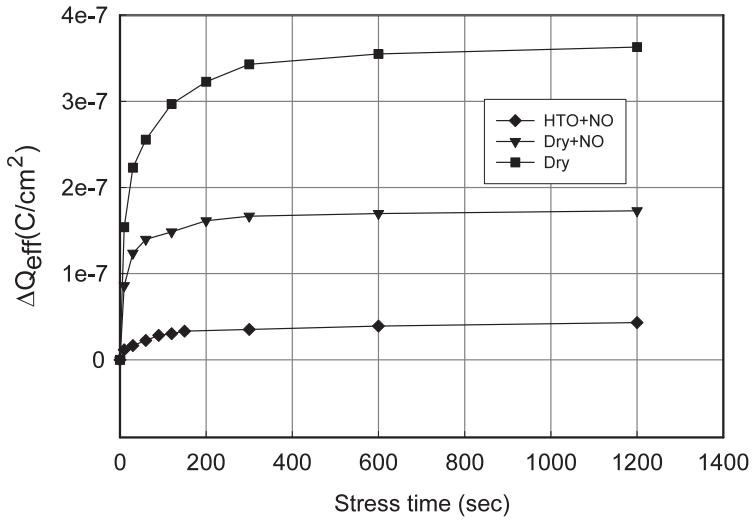

Figure 10. The change of effective oxide charge with charge injection time.

state density following the NO anneal. The passivation process improves the oxide hot-carrier tolerance as well.

4. Modelling of the nitrogen passivation

The areal density of ^{15}N at the SiO_2/SiC interface was measured by nuclear reaction analysis (NRA) using the $^{15}N(p, \alpha)$ 12C reaction at $E_p = 1$ MeV. Figure 11 shows ^{15}N areal densities at the interface in SiO_2/SiC following ^{15}NO passivation anneals at temperatures from 1050 to 1175 °C. The nitrogen content initially increases with time and the incorporation rate increases with temperature. At temperatures above 1050 °C, the initial nitrogen incorporation is followed by the removal of nitrogen from the oxide. The nitrogen content then saturates at a temperature-independent value of $\sim 1.6 \times 10^{14}$ cm^{-2}. The SIMS depth profiles in figure 12 show that nitrogen is concentrated only at the interface and new oxide growth occurs in the substrate in NO anneals. The nitridation of SiO_2/SiC proceeds by two competing processes: (1) NO reacts with defects at the interface to incorporate nitrogen, and (2) O_2 produced by the thermal decomposition of NO oxidizes the substrate and removes nitrogen from the interface. Initially, the nitridation reaction is faster than oxidation and results in an increase in nitrogen content. After a temperature-dependant time, the nitridation and oxidation reactions begin to equalize, and the nitrogen content decreases. Eventually, the nitridation and oxidation reactions reach equilibrium, and the nitrogen content saturates as the oxide thickness increases [40].

The relationship between nitrogen content and interface density in SiO_2/SiC near the conduction band has been investigated quantitatively and a model for the nitrogen passivation of these traps has been suggested [41]. In this model, each interface defect is a cluster of atoms that introduces a trap level near the conduction band of 4H-SiC. The energy of this state corresponds directly to the size of the cluster, with the largest cluster at the highest energy. These clusters vary in size and produce a series of associated trap levels in the band gap. When an atom in a cluster is passivated with a nitrogen atom, it is removed from the cluster. The passivated atom then introduces a trap state in or near the valence band, and the energy of the remaining cluster is shifted lower in the band gap by one trap level. During nitridation,

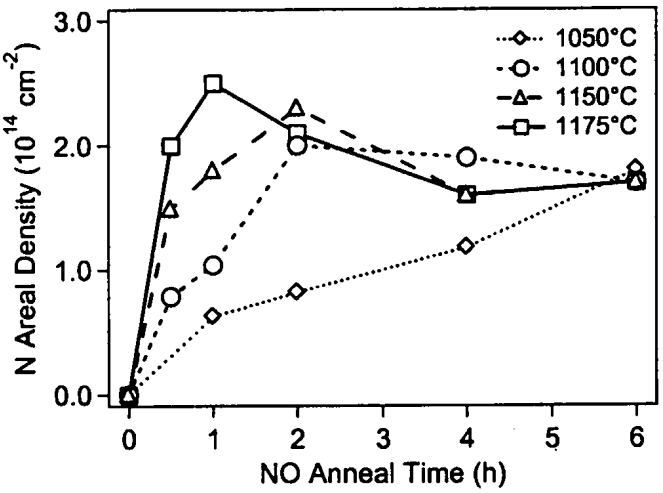

Figure 11. ^{15}N content in SiO_2/SiC after annealing in ^{15}NO at 100 Torr, at temperatures from 1050 to 1175 °C.

therefore, the trap density in an energy level decreases when a cluster in that level is passivated and increases from the 'feeding in' process when a cluster in the level above is passivated.

The total interface trap density D_{it} at an energy E as a function of nitrogen content N is given by

$$D_{it}(E; N) = L(E) + T_0(E)^{e-R(E)N} \sum_{j=0}^{n(E)} \frac{(R(E)N)j}{J!}. \tag{1}$$

The parameter L represents noncluster traps that are not passivated by nitrogen and cause the observed D_{it} saturation at high nitrogen amounts. The sum limit n represents the number of cluster levels above the energy E, not the size of the cluster at energy E. The parameters T_0 and R are the initial trap density and passivation cross section, respectively, at energy E.

Figure 13 shows interface trap density as a function of nitrogen areal density at energies 0.2–0.6 eV from the conduction band fitted using equation (1). The fits to the data are excellent for all energies. The traps at lower energies are passivated relatively quickly, but since the trap density is larger at higher energies, traps are feeding in at the same rate as they are being passivated out of a level. The trap density in a level therefore remains nearly constant until the higher-energy levels are completely passivated, and it is only at this point that the trap density decreases. This process causes the nitrogen passivation threshold seen at $\sim 10^{14}$ cm^{-2}. This model also provides a simple explanation for the need for $\sim 2.5 \times 10^{14}$ cm^{-2} of nitrogen to passivate a trap density of $\sim 10^{12}$ cm^{-2}. The dissolution process implies that complete passivation requires one nitrogen atom for each atom in the cluster. The sum of all atoms in all defect clusters available for passivation is evidently $\sim 2.5 \times 10^{14}$ cm^{-2}, which is consistent with the amount of excess silicon or carbon at the interface.

5. Conclusions

A nitric oxide passivation process has been developed for 4H-SiC MOSFETs. We have observed that for dry oxides, wet oxides, thin oxides (~18 nm), thick oxides (400 nm), HTO

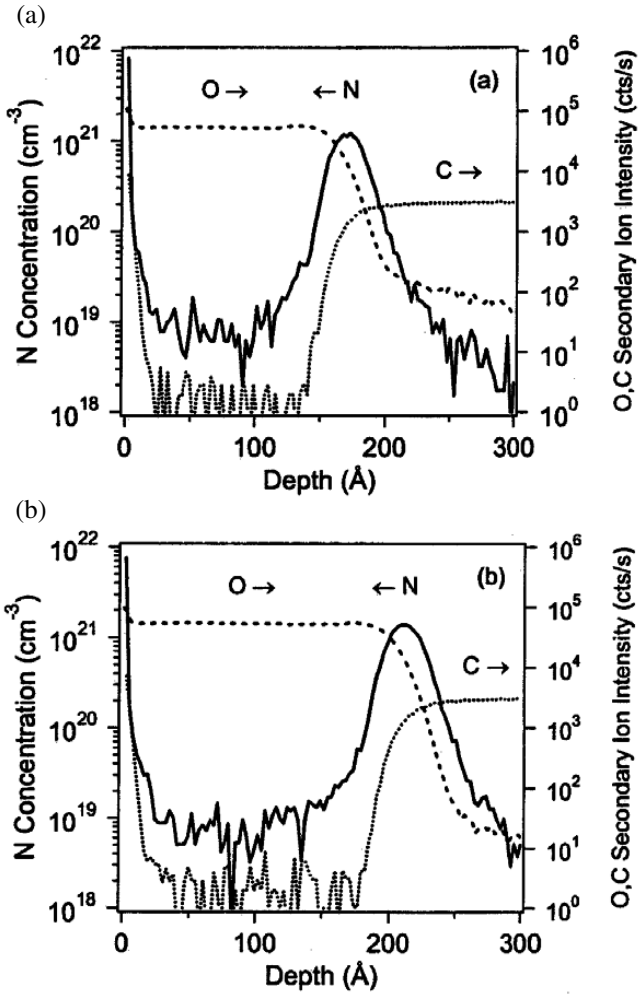

Figure 12. SIMS profiles of SiO_2/SiC annealed in NO at 1150 °C at 1 atm for (a) 0.5 h and (b) 4 h. The oxide depths are (a) 164 and (b) 203.

and LTO, our optimized NO passivation process results in an interface state density of around 1×10^{12} cm^{-2} eV^{-1} for n-4H-SiC at $E_c - E = 0.15$ eV regardless of initial oxide growth or deposition processes. Our supposition is that the passivation anneal produces a thin thermal oxide at the interface where defect passivation by nitrogen and defect generation as a result of the continuing oxidation are competing processes. This supposition regarding oxide growth during the NO passivation anneal raises the question of whether nitrogen can be supplied at the SiO_2/SiC interface without additional oxide growth. Passivation at lower temperatures with atomic nitrogen is one possibility, and studies are currently under way.

The NO passivation process improves the field effect channel mobility to 35–50 cm^2 V^{-1} s^{-1} and the low field mobility to above 100 cm^2 V^{-1} s^{-1} at room temperature. Field effect mobilities for all devices show positive temperature dependence; however, passivated MOSFETs have much weaker dependence by comparison. Threshold voltages decrease with increasing temperature because of the liberation of electrons trapped at acceptor-

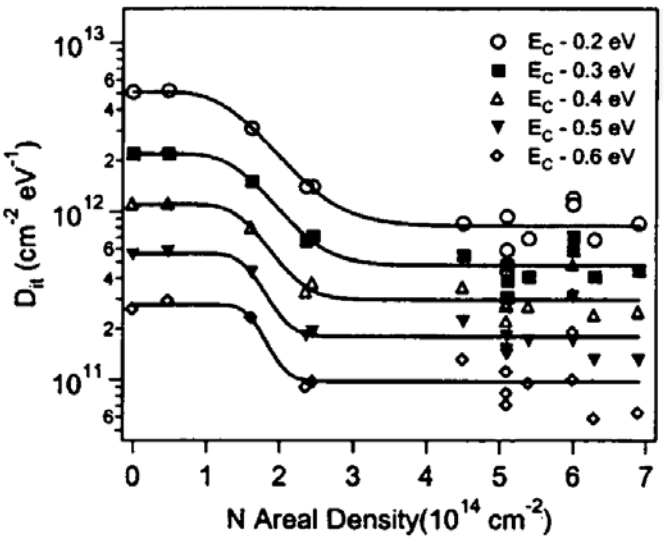

Figure 13. Interface trap density D_{it} as a function of nitrogen areal density at energies 0.2–0.6 eV from the conduction band E_c fitted using equation (1).

like defects near the conduction band edge. Nitric oxide passivation significantly reduces the shift in V_{th} at higher temperatures. Increased mobility and lower threshold voltage at higher temperatures are consistent with the liberation of electrons trapped near the conduction band edge. Mobility increases as the result of reduced Coulomb scattering, and V_{th} decreases because there is less negative charge at the SiC–SiO_2 interface. The hot-carrier tolerance of the 4H-MOS capacitors passivated with NO was investigated using reliability tests based on the charge injection method. The hot-carrier tolerance showed a similar behaviour to the interface state density following NO passivation, and NO passivated oxides had better reliability.

The nitrogen content initially increases with time and temperature of NO anneal, but nitrogen is removed at later times at temperatures above 1050 °C. This nitrogen removal, and the associated oxide growth in the SiC substrate, is caused by O_2 formed by the thermal decomposition of NO. Eventually the nitridation and oxidation reactions reach equilibrium, and the nitrogen content saturates as the oxide thickness increases. The NO passivation effect saturates after $\approx 2.5 \times 10^{14}$ cm^{-2} of nitrogen at the interface. These results are consistent with a model of the interface in which defects such as carbon clusters or silicon sub-oxide states produce traps with energies corresponding to the sizes of the defects. Nitrogen passivation results in the dissolution of the defects, which then lowers the trap energies in the band gap.

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